In th Sp cificati n

On page 27, the Abstract, spanning lines 2 through 20, has been replaced with the paragraph shown below.

Semiconductor processing methods of forming transistors and related integrated circuitry are described. In one embodiment, a plurality of shallow trench isolation regions are formed within a substrate and define a plurality of active areas having widths at least some of which being no greater than about one micron, with some of the widths preferably being different. A gate line is formed over the respective active areas to provide individual transistors, with the transistors corresponding to the active areas having the different widths having different threshold voltages.

In the Claims

21. A semiconductor processing method comprising forming two series of field effect transistors over a substrate, one series being isolated from adjacent devices by shallow trench isolation, the other series having active area widths greater than one micron, the one series being formed to have active area widths less than one micron to achieve lower threshold voltages than the other of the series.

22. The semiconductor processing method of claim 21, wherein the threshold voltages for the two series of field effect transistors are defined by a common chann l implant.